(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 645 811 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **94115009.6**

(51) Int. Cl.[6]: **H01L 23/057**, H01L 23/367

(22) Date of filing: **23.09.94**

(30) Priority: **24.09.93 JP 238144/93**

(43) Date of publication of application:
29.03.95 Bulletin 95/13

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **KABUSHIKI KAISHA TOSHIBA**
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi
Kanagawa-ken 210 (JP)

(72) Inventor: **Kozono, Hiroyuki, c/o Intellectual Property Div.**
Kabushiki Kaisha Toshiba,
1-1 Shibaura 1-chome
Minato-ku,
Tokyo 105 (JP)

(74) Representative: **Lehn, Werner, Dipl.-Ing. et al**
Hoffmann, Eitle & Partner,
Patentanwälte,
Arabellastrasse 4
D-81925 München (DE)

(54) Semiconductor device having semiconductor chip with backside electrode.

(57) A semiconductor chip (11) is mounted on a chip-mounting section (12). A conduction path forming section (20) having a plurality of conduction paths (24) formed therein is placed around the chip-mounting section (12). A heat sinking board (14) is bonded to the backsides of the chip-mounting section (12) and the conduction path forming section (20). In the conduction path forming section (20), a second insulating layer (22) is formed with notches (25), whereby the exposed area of conduction paths (24) that are wire-bonded to the chip-mounting section (12) is increased.

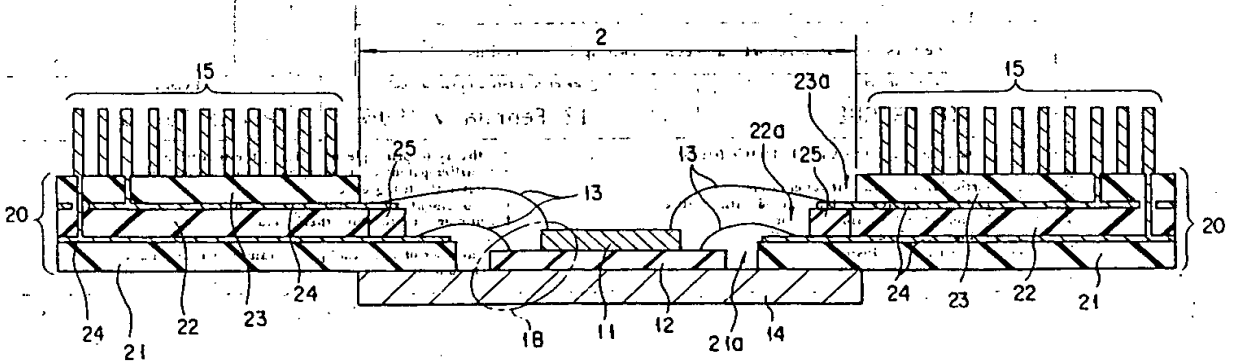


FIG. 1A

EP 0 645 811 A2

The present invention relates to a semiconductor device and more particularly to a semiconductor device in which an electrode is drawn out of the backside of an on-board semiconductor chip.

As a form of package used for semiconductor integrated circuits there is a PGA (pin grid array). The PGA is arranged such that external terminals or pins are fixed to a package body at regular intervals vertically and in the form of grid. The PGA is often used as a multi-terminal package.

Semiconductor devices used in high frequency bands each have an electrode formed on the entire backside of their respective semiconductor chip in order to stabilize their operating characteristics. Hereinafter, such an electrode is referred to as a backside electrode.

FIG. 6 shows a conventional semiconductor device having a PGA structure. In FIG. 6, the semiconductor device comprises a semiconductor chip 101, a chip-mounting section 102, a conducting path forming section 110, a plurality of bonding wires 103, a heat sinking board 104, and a plurality of pin-like external terminals 112. The semiconductor chip 101 has an electrode formed on its backside. The semiconductor chip 101 is mounted on the chip-mounting section 102. The conducting path forming section is disposed around the edges of the chip-mounting section 102 and have a plurality of conducting paths 111 formed inside. The bonding wires 103 connect pad electrodes (not shown) formed on the semiconductor chip 101 and the chip-mounting section 102 to corresponding respective ones of the conduction paths 111. The heat sink 104 is bonded to the backside of each of the chip-mounting section 102 and the conductive-path forming section 110. The chip-mounting section 102 is made of an insulating material and coated on top with a conductive film, not shown. The external terminals 112 are provided on the top of the conducting path forming section 110 and electrically connected to the respective ones of the conduction paths 111.

FIG. 7 is an enlarged view of the semiconductor chip 101, the chip-mounting section 102, and the conduction path forming section 110. In this FIGURE, the conduction paths 111 are provided radially on first and second insulating layers 113 and 114. Each of pad electrodes 115 on the semiconductor chip 101 is connected to a respective one of the conduction paths 111 by a bonding wire 103. The backside electrode of the semiconductor chip 101 is electrically connected to the conductive film 102a on the top of the chip-mounting section 102, which, in turn, is connected to a conduction path 111a on the first insulating layer 113 by bonding wires 103.

It is thus required that the conductive film 102a on the chip-mounting section 102 be wire-bonded to the conduction path 111a when the semiconductor chip 101 is coated underneath with an electrode. In this case, as shown in FIG. 7, this wire bonding is performed at corners of the chip-mounting section 102 and the conduction path forming section 110, which offers little obstruction to wire bonding of the pad electrodes on the chip and allows the bonding area to be increased.

The reliability of semiconductor devices is significantly affected by wire bonding. Thus, good bonding must be effected at all connection points. In general, however, there is a tendency that, when a wire used is short, the resulting wire loop becomes low in height and, when a wire used is too long, it comes loose to form an underloop. In other words, the bonding wires must lie within an appropriate range of length. When a wire is short, it is liable to peel off the point where it has been bonded. When a wire is too long, on the other hand, it may come in contact with another portion. For this reason, the length of the bonding wires between the conductive film 102a on the chip-mounting section 102 and the conduction path 111a must be set appropriately.

The wire bonding is performed by the use of a capillary and hence there is a need for a space where it can move. In wire bonding for the semiconductor chip 101 and the conduction path 111a in particular, the space where the capillary moves must be fully taken into consideration because the semiconductor chip 101 or the second insulating layer 114 of the conduction path forming section 110 forms a difference in level within the space for movement of the capillary. That is, assuming the shortest distance between a point of bonding on the conductive film 102a and the corner of the semiconductor chip to be L1 and the shortest distance between a point of bonding on the conduction path 111a and the corner of the second insulating layer 114 to be L2, these distances L1 and L2 must be set to the shortest distance required for bonding over which the capillary can move. Thus, the size W of the cavity shown in FIG. 6, or the inside diameter of the conductive path forming section 110, is defined by the size of the semiconductor chip 101 and the space needed for wire bonding at the corners.

FIG. 8 shows cavity size versus semiconductor chip size. When no wire bonding is performed on the chip-mounting section 102 and the conduction path forming section 110, the semiconductor chip size is allowed to lie in the range defined by lines A1 and A2. When wire bonding is performed, on the other hand, the chip size must lie within the range defined by lines A1 and A3. To be specific, assume that the cavity size is 10 mm. If, in this case, no wire bonding is performed, the semiconductor chip size can range from 4.0 to 7.0 mm.

When wire bonding is performed, the chip size must range from 4.0 to 5.0 mm. That is, when the chip-mounting section 102 and the conduction path forming section 110 need to be connected with each other by wire bonding, the chip size is restricted within narrow limits, decreasing the versatility of the conduction path forming section (cavity) 110 or the semiconductor chip 101.

As described above, since the chip-mounting section 102 and the conduction path forming section 110 are wire bonded so as to connect the backside electrode of the semiconductor chip and the conduction path forming section 110 with each other, a space must be reserved for wire bonding. This restricts the size of a semiconductor chip.

It is an object of the present invention to provide a PGA-structured semiconductor device which has an on-board semiconductor chip with a backside electrode and permits the size of the semiconductor chip to be increased.

According to a first aspect of the present invention, there is provided a semiconductor device comprising:

a semiconductor chip having a plurality of pad electrodes on its top and a backside electrode on its backside;

a chip-mounting section on which the semiconductor chip is mounted, the chip-mounting section having a conductive layer on its top which is in contact with the backside electrode of the semiconductor chip;

a conduction path forming section disposed around the chip-mounting section, the conduction path forming section including first, second and third insulating layers, the second insulating layer being located over the first insulating layer, the third insulating layer being located over the second insulating layer, the first, second and third insulating layers having their respective openings which increase in diameter in the order of the first, second and third insulating layers, the semiconductor chip being placed in the opening of the first insulating layer; a plurality of external terminals arranged on the third insulating layer; a first group of conduction paths formed on the first insulating layers and having their one ends exposed in the opening of the second insulating layer and their other ends connected to the external terminals; and a second group of conduction paths formed on the second insulating layer and having their one ends exposed in the opening of the third insulating layer and their other ends connected to the external terminals;

a first group of bonding wires for electrically connecting the one ends of the first group of conduction paths with the conductive layer of the chip-mounting section;

a second group of bonding wires for electrically connecting the one ends of the second group of conduction paths with the pad electrodes of the semiconductor chip; and

a heat sinking board bonded to the backside of the chip-mounting section and part of the backside of the conduction path forming section,

the second insulating layer having notches which are cut in the opposite direction to the semiconductor chip, and the exposed area of the first group of conduction paths being set larger than that of the second group of conduction paths.

According to a second aspect of the present invention, there is provided a semiconductor device comprising:

a semiconductor chip having a plurality of pad electrodes on its top and a backside electrode on its backside;

a conduction path forming section disposed around the semiconductor chip, the conduction path forming section including first, second and third insulating layers, the second insulating layer being located over the first insulating layer, the third insulating layer being located over the second insulating layer, the first, second and third insulating layers having their respective openings which increase in diameter in the order of the first, second and third insulating layers, the semiconductor chip being placed in the opening of the first insulating layer; a plurality of external terminals arranged on the third insulating layer; a first group of conduction paths formed on the first insulating layers and having their one ends exposed in the opening of the second insulating layer and their other ends connected to the external terminals; a second group of conduction paths formed on the second insulating layer and having their one ends exposed in the opening of the third insulating layer and their other ends connected to the external terminals; and a conductor formed in the first insulating layer and having its one end connected to the first group of conduction paths and its other end exposed on the backside of the first insulating layer;

a chip-mounting section provided on the backside of the first insulating layer and coated on top with a conduction layer on which the semiconductor chip is mounted, the backside electrode of the semiconductor chip and the other end of the conductor in the first insulating layer being connected together by the conduction layer;

bonding wires for electrically connecting the one ends of the second group of conduction paths with the pad electrodes of the semiconductor chip; and

a heat sinking board bonded to backsides of the chip-mounting section and the first insulating layer.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in

which:

FIG. 1A is a diagrammatic sectional view of a semiconductor device according to a first embodiment of the present invention;

FIG. 1B is an enlarged view of a portion indicated by circle 1B in FIG. 1A;

FIG. 2 is a plan view of a portion corresponding to line 2 in FIG. 1A;

FIG. 3 is an enlarged perspective view of a portion indicated by circle 3 in FIG. 2;

FIG. 4A is a diagrammatic sectional view of a semiconductor device according to a second embodiment of the present invention;

FIG. 4B is an enlarged view of a portion indicated by circle 4B in FIG. 4A;

FIG. 5A is a diagrammatic sectional view of a semiconductor device according to a third embodiment of the present invention;

FIG. 5B is an enlarged view of a portion indicated by circle 5B in FIG. 5A;

FIG. 6 is a diagrammatic sectional view of a conventional semiconductor device;

FIG. 7 is an enlarged sectional view of a portion of the semiconductor device of FIG. 6; and

FIG. 8 is a graph illustrating a relationship between the semiconductor chip size and the cavity size.

FIGS. 1A and 1B show a semiconductor device according to a first embodiment of the present invention. The semiconductor device comprises a semiconductor chip 11, a chip-mounting section 12, a conduction path forming section 20, bonding wires 13, a heat sinking board 14, and pin-like external terminals 15. The semiconductor chip 11 is mounted on the chip-mounting section 12. The conduction path forming section 20 is disposed around the chip-mounting section 12 and has a plurality of conduction paths 24 formed inside. The bonding wires 13 electrically connect pad electrodes (not shown) on the semiconductor chip 11 and the chip-mounting section 12 with the conduction paths 24. The heat sink 14 is bonded to the backsides of the chip-mounting section 12 and the conduction path forming section 20. The external terminals 15 are provided on the top of the conduction path forming section 20.

The conduction path forming section 20 comprises a first insulating layer 21, a second insulating layer 22, a third insulating layer 23, and conduction paths 24 interposed between every insulating layer. The first, second and third insulating layers 21, 22 and 23 respectively have square openings 21a, 22a and 23a each having a different diameter. Of these openings, the uppermost opening 23a is the greatest in diameter, followed by the opening 22a. Thus, the insulating layers 21, 22 and 23 form steps at their central portion. The second insulating layer 22 has notches 25 formed at the four corners of the square opening 22a. The notches will be described later in detail. Each of the conduction paths has its end exposed at the opening and its other end electrically connected to a corresponding one of the external terminals 15.

FIG. 1B is an enlarged view of a portion indicated by circle 1B in FIG. 1A. The semiconductor chip 11 has a backside electrode 11a produced by metal evaporation onto its backside. The chip-mounting section 12 consists of a highly insulating material and is coated on top with a metal layer 121. The backside of the semiconductor chip 11 is bonded to the metal layer 121 by a conductive adhesive 16. The heat sink 14 is bonded to the backside of the chip-mounting section 12 by an adhesive 17. This adhesive 17 may be either insulating or conducting. The heat sink 14 is also bonded to the backside of the conduction path forming section 20 by the adhesive 17.

FIG. 2 is a plan view of a portion corresponding to line 2 in FIG. 1A with bonding wires 13 omitted on the left side of a diagonal dashed-and-dotted line. As can be seen from this figure, the conduction paths 24 extend radially on the first and second insulating layers 21 and 22. The second insulating layer 22 is formed at its respective corners with notches 25. Each notch is formed in the opposite direction to a corresponding one of the corners of the semiconductor chip 11.

The notches 25 will be further described with reference to FIG. 3. The notches 25 are formed at the corners of the second insulating layer 22. Each notch increases the exposed area of the conduction path 24a formed on the first insulating layer 21. One of the bonding wires 13 has its one end bonded to the metal layer 121 and its other end bonded to that portion of the conduction path 24a which is exposed by the notch 25. This permits the bonding wire 13 to be set to an appropriate length. Moreover, the point of bonding on the chip-mounting section 12 can be put away from the semiconductor chip 11, permitting the distance L1 to be set long. Thus, the metal layer 121 and the conduction path 24a can be readily connected to each other by wires. In addition, the distance L2 can also be set long, which permits a sufficient space to be reserved for movement of the capillary. Furthermore, since the notches 25 are formed at the corners of the second insulating layer 22, the pad electrodes 27 on the semiconductor chip 11 and the conduction paths 24 on the second insulating layer 22 can be connected together by bonding wires 13 in the same manner as the prior art.

Here, L1 is the shortest distance between the point of bonding on the chip-mounting section 12 and the semiconductor chip 11, and L2 is the distance between the point of bonding on the conduction path 24a and the intersection of a straight

line along the bonding wire and the second insulating layer 22, i.e., the distance between the point of bonding on the conduction path 24a and the deepest point in the notch 25.

According to the first embodiment of the present invention, the notches 25 are provided at the corners of the square opening 22 in the second insulating layer 22 to thereby increase the exposed area of the conduction path 24a that is wire-bonded to the chip-mounting section 12. Thus, the space for movement of the capillary can be increased, thereby permitting easy bonding. In addition, the bonding wires can be set to an appropriate length, which prevents the wires from peeling off.

Since the exposed area of the conduction path 24a is increased, the points of bonding on the chip-mounting section 12 can be put away from the semiconductor chip even if the length of the bonding wires is set appropriately. For this reason, increasing the semiconductor chip size is allowed.

In the first embodiment, the notches 25 are provided at the corners of the second insulating layer 22. This is not restrictive. The notches may be provided at other portions of the second insulating layer than its corners if they are located over the conduction paths 24a. In other words, the conduction paths 24a can be located in any position on the first insulating layer 21 where they do not come into contact with other bonding wires, and the notches 25 can be formed on such conduction paths.

Next, reference will be made to FIGS. 4A and 4B to describe a second embodiment of the present invention. In FIGS. 4A and 4B, like reference numerals are used to denote corresponding portions to those in the first embodiment, and only different portions will be described below.

In FIG. 4A, the semiconductor chip 11 is mounted on the chip-mounting section 12 by means of a conductive adhesive (not shown). The first insulating layer 21 is undercut along its opening 21a to form an undercut portion 26. The periphery of the chip-mounting section 12 is fit into the undercut 26 of the insulating layer 21. The backsides of the chip-mounting section 12 and the conduction path forming section 20 are bonded to the heat sink 14 by means of an insulating adhesive (not shown).

FIG. 4B is an enlarged view of a portion indicated by circle 4B in FIG. 4A. In FIG. 4B, the first insulating layer 21 is formed with a conduction path 24b which passes through that layer and is connected with the conduction path 24b on the first insulating layer 21. The metal layer 121 provided on the top of the chip-mounting section 12 and the conduction path 24b are electrically connected with each other by means of conductive adhesive 16. That is, the backside electrode of the semiconductor chip 11 is electrically connected to the conduction path 24a through the metal layer 121, conductive adhesive 16 and conduction path 24b without using wire bonding.

It is needless to say that the pad electrodes (not shown in FIGS. 4A and 4B) on the semiconductor chip 11 are connected by bonding wires to the conduction paths radially arranged on the first insulating layer 21 or second insulating layer 22.

Next, a third embodiment of the present invention will be described with reference to FIGS. 5A and 5B. Like reference numerals are used to denote corresponding parts to those in the second embodiment. The present embodiment uses an insulating heat sinking board 30, which serves as a chip-mounting section and a heat sink. A metal layer 121 is deposited onto the top of the insulating heat sinking board 30, and the semiconductor chip 11 is bonded to the metal layer 121 by a conductive adhesive not shown.

FIG. 5B is an enlarged view of a portion indicated by circle 5B in FIG. 5A. The insulating heat sinking board 30 has a stepped portion 31 along its periphery. The stepped portion 31 of the heat sinking board 30 is fit into the undercut portion 26 of the first insulating layer 21 and they are bonded to each other by a conductive adhesive 19. The backside electrode (not shown) of the semiconductor chip 11 is electrically connected to the conduction path 24a through the conductive adhesive 16, metal layer 121, conductive adhesive 19 and conduction path 24b.

In the second embodiment, the conduction path forming section 20 and the chip-mounting section 12 are electrically connected together by the conductive adhesive 16, and, in the third embodiment, the conduction path forming section 20 and the insulating heat sinking board 30 are electrically connected together by the conductive adhesive 19. That is, the second and third embodiments eliminate the need for the metal layer 121 and the conduction path 24a to be wire-bonded together as in the first embodiment. Thus, there is no restriction on semiconductor chip size. Namely, the chip size can be increased. The use of a semiconductor chip about the size of a cavity is allowed. Also, the semiconductor chip size can be made substantially the same as when no electrode is drawn out of the backside of the chip.

Claims

1. A semiconductor device characterized by comprising:

a semiconductor chip (11) having a plurality of pad electrodes (115) on its top and a backside electrode (11a) on its backside;

a chip-mounting section (12) on which said semiconductor chip is mounted, said chip-

mounting section having a conductive layer (121) on its top which is in contact with said backside electrode of said semiconductor chip;

a conduction path forming section (20) disposed around said chip-mounting section (12), said conduction path forming section including first, second and third insulating layers (21, 22, 23), said second insulating layer (22) being located over said first insulating layer (21), said third insulating layer (23) being located over said second insulating layer, said first, second and third insulating layers having their respective openings (21a, 22a, 23a) which increase in diameter in the order of said first, second and third insulating layers, said semiconductor chip (11) being placed in said opening of said first insulating layer (21); a plurality of external terminals (15) arranged on said third insulating layer (23); a first group of conduction paths (24) formed on said first insulating layer (21) and having their one ends exposed in said opening of said second insulating layer (22) and their other ends connected to said external terminals (15); and a second group of conduction paths (24) formed on said second insulating layer (22) and having their one ends exposed in said opening of said third insulating layer (23) and their other ends connected to said external terminals (15);

a first group of bonding wires (13) for electrically connecting said one ends of said first group of conduction paths (24) with said conductive layer (121) of said chip-mounting section (12);

a second group of bonding wires (13) for electrically connecting said one ends of said second group of conduction paths (24) with said pad electrodes (115) of said semiconductor chip (11); and

a heat sinking board (14) bonded to said backside of said chip-mounting section (12) and part of the backside of said conduction path forming section (20),

said second insulating layer (22) having notches (25) which are cut in the opposite direction to said semiconductor chip (11), and the exposed area of said first group of conduction paths (24) being set larger than that of said second group of conduction paths (24).

2. A device according to claim 1, characterized in that each of said openings (21a, 22a, 23a) of said first, second and third insulating layers is square, and said notches (25) are formed at corners of said opening of said second insulating layer (22).

3. A device according to claim 1, characterized in that said first group of bonding wires (13) have their one ends bonded to those parts of said first group of conduction paths (24a) which are exposed in said notches (25) and their other ends bonded to said conduction layer (121) of said chip-mounting section (12).

4. A semiconductor device characterized by comprising:

a semiconductor chip (11) having a plurality of pad electrodes (115) on its top and a backside electrode (11a) on its backside;

a conduction path forming section (20) disposed around said semiconductor chip, said conduction path forming section (20) including first, second and third insulating layers (21, 22, 23), said second insulating layer (22) being located over said first insulating layer (21), said third insulating layer (23) being located over said second insulating layer (22), said first, second and third insulating layers having their respective openings (21a, 22a, 23a) which increase in diameter in the order of said first, second and third insulating layers, said semiconductor chip (11) being placed in said opening of said first insulating layer; a plurality of external terminals (15) arranged on said third insulating layer (23); a first group of conduction paths (24) formed on said first insulating layer (21) and having their one ends exposed in said opening of said second insulating layer (22) and their other ends connected to said external terminals (15); a second group of conduction paths (24) formed on said second insulating layer (22) and having their one ends exposed in said opening of said third insulating layer (23) and their other ends connected to said external terminals (15); and a conductor (24b) formed in said first insulating layer (21) and having its one end connected to said second group of conduction paths (24) and its other end exposed on the backside of said first insulating layer (21);

a chip-mounting section (12) provided on the backside of said first insulating layer (21) and coated on top with a conductive layer (121) on which said semiconductor chip (11) is mounted, said backside electrode (11a) of said semiconductor chip (11) and the other end of said conductor (24b) in said first insulating layer being connected together by said conductive layer (121);

bonding wires (13) for electrically connecting said one ends of said second group of conduction paths (24) with said pad electrodes (115) of said semiconductor chip (11); and

a heat sinking board (14) bonded to back-

sides of said chip-mounting section (12) and said first insulating layer (21).

5. A device according to claim 4, characterized in that said first insulating layer (21) has an undercut portion (26) formed along its opening, and the other end of said conductor (24a) in said first insulating layer is exposed in said undercut portion.

6. A device according to claim 5, characterized in that the periphery of said chip-mounting section (12) is fit into said undercut portion (26) of said first insulating layer (21), and the other end of said conductor (24a) is in contact with said conductive layer (121) of said chip-mounting section at said undercut portion.

7. A device according to claim 4, characterized in that said chip-mounting section (12) and said heat sinking board (14) have insulating and heat sinking properties and are formed integral with each other.

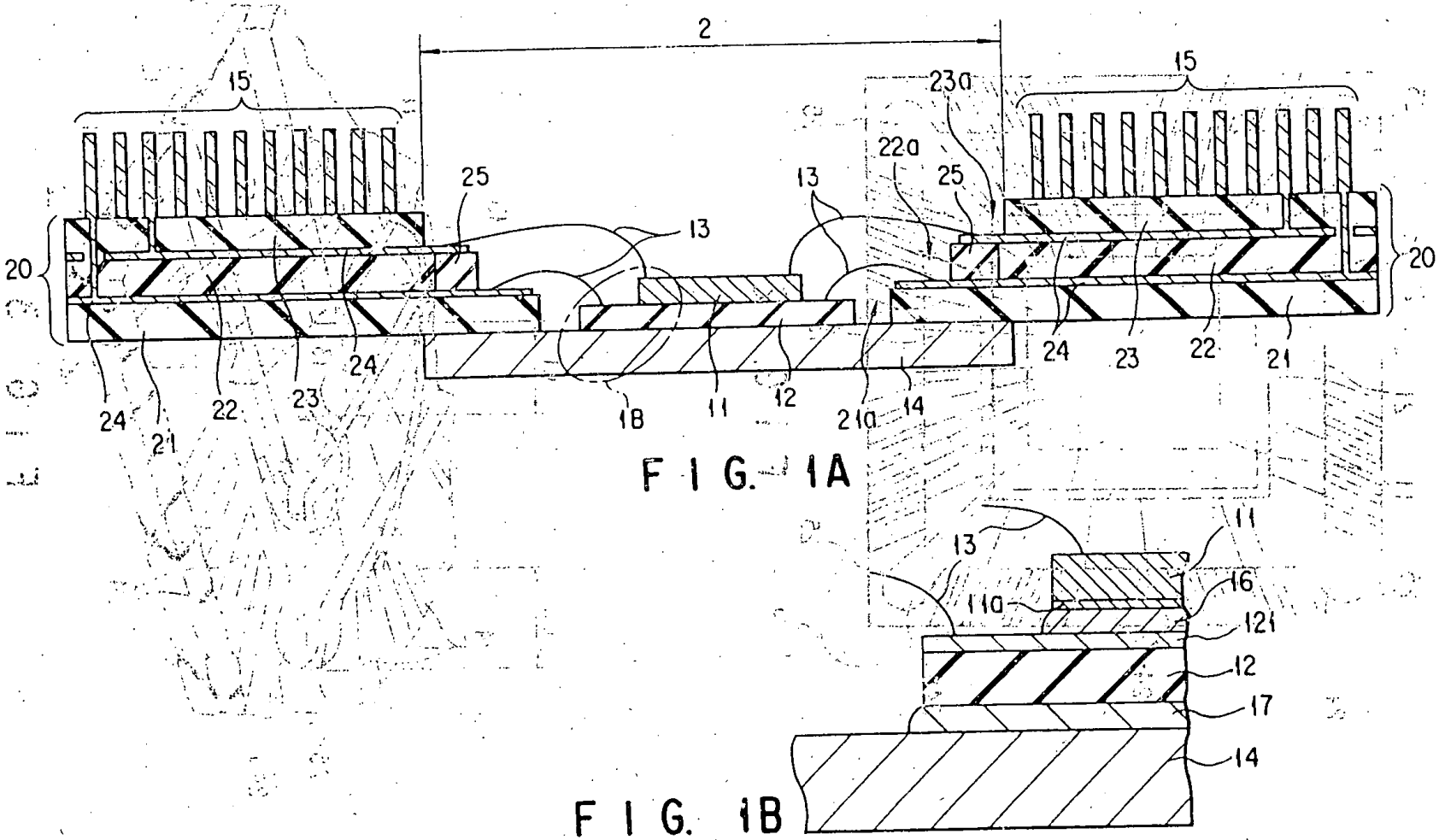

2
15
15
230
220
25
25
13
13
20
20
24
21
22
23
24
18
11
12
210
14
24
23
22
21

FIG. 1A

13
11
16
110
121
12
17
14

FIG. 1B

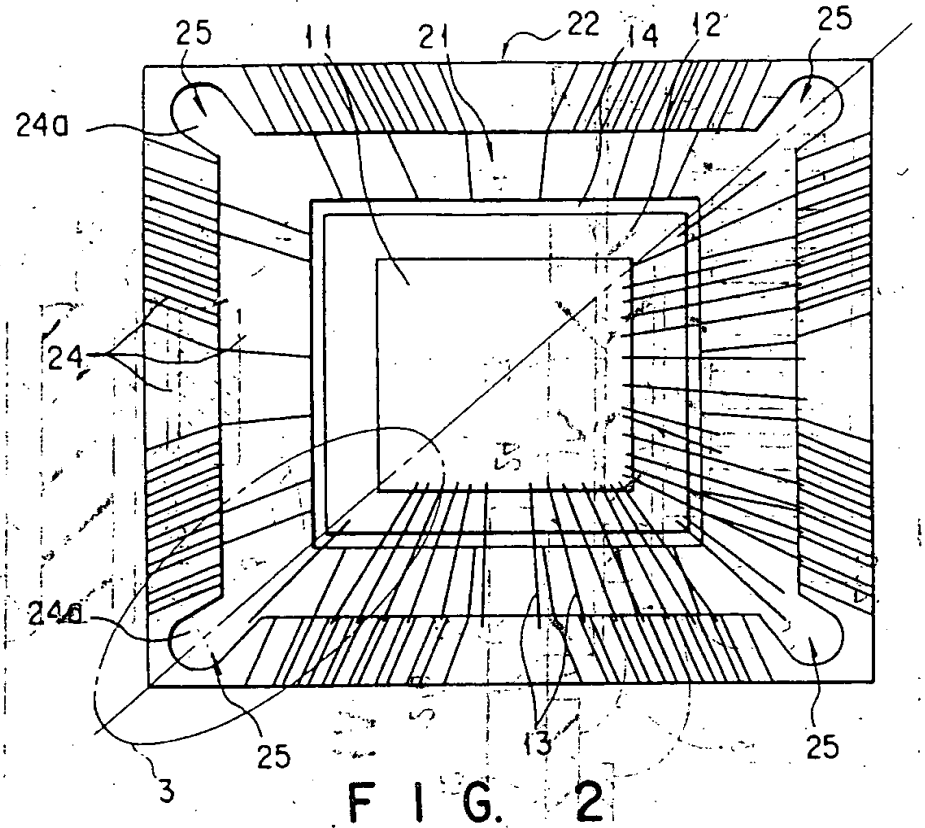

25
11
21
22
14
12
25
240
24
240
25
25
3
13

FIG. 2

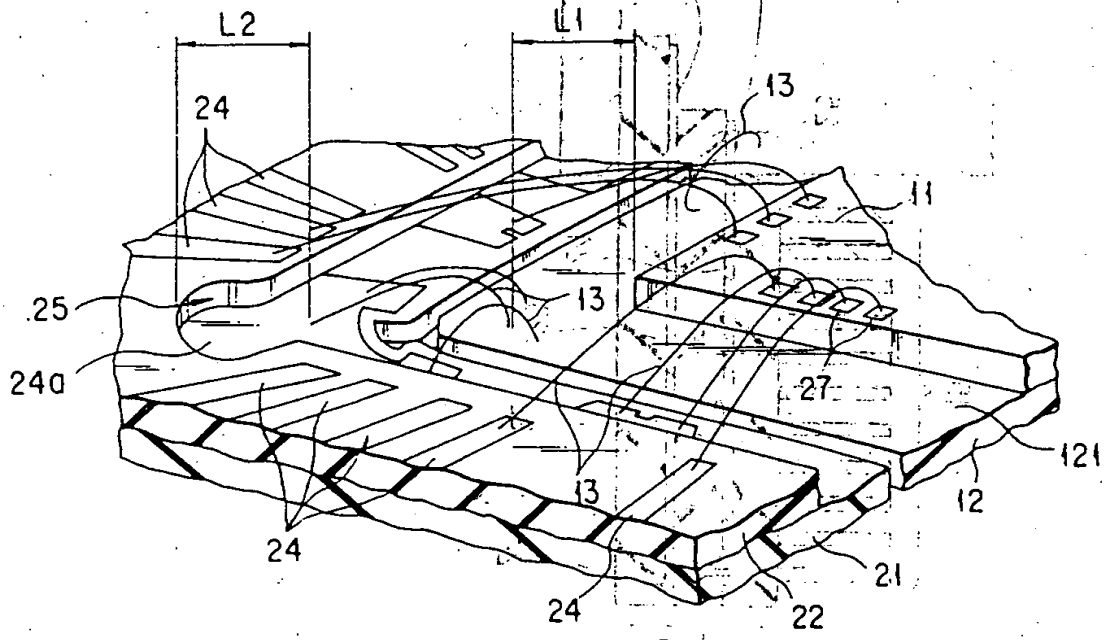

L2
L1
24
13
11
25
13
240
27
121
13
12
24
21
24
22

FIG. 3

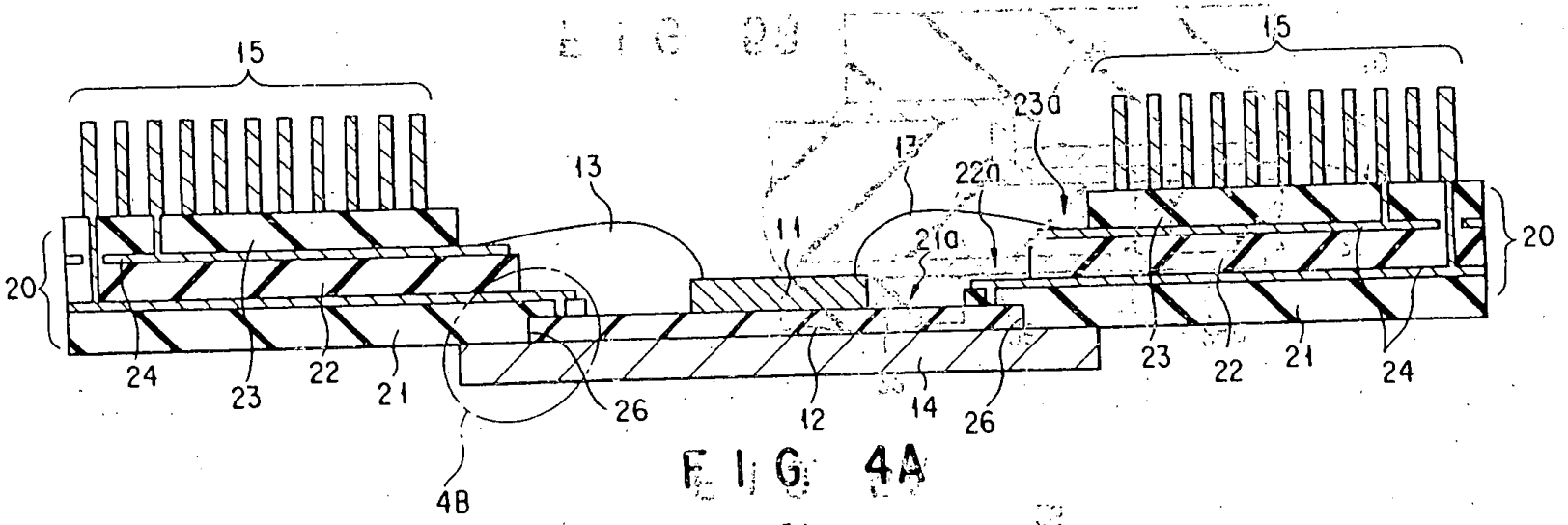

15
15
230
13
17
220
11
210
20
20
24
23
22
21
26
12
14
26
23
22
21
24
4B

FIG. 4A

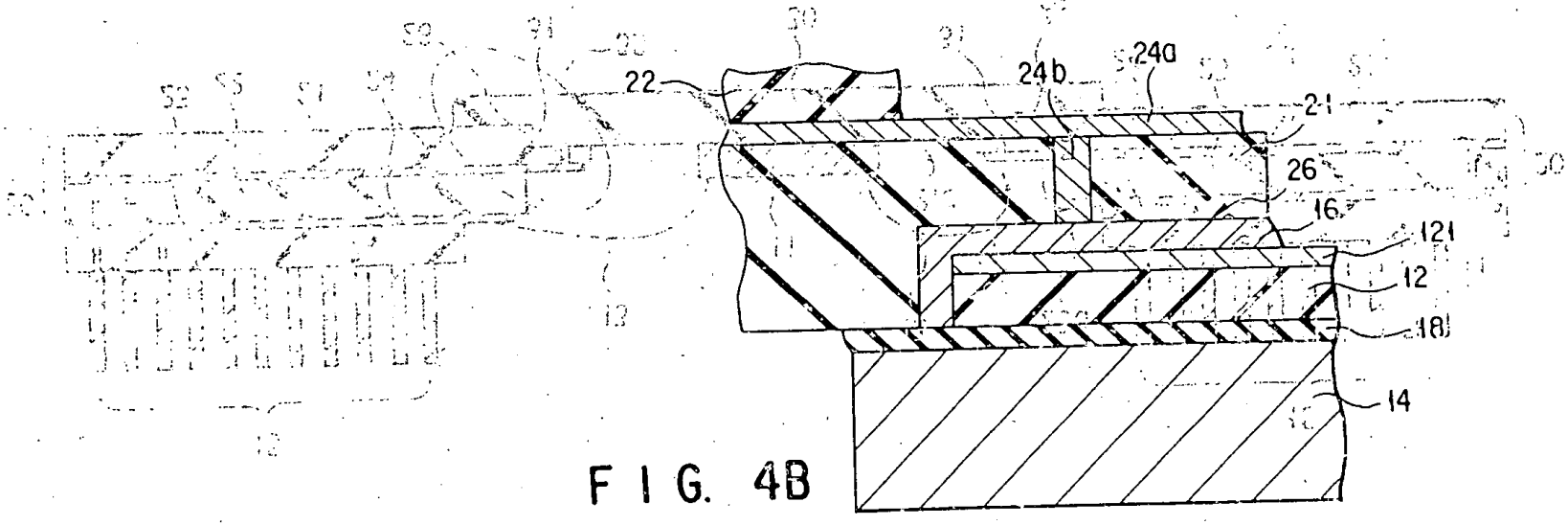

22
24b
240
21
26
16
121
12
18
14

FIG. 4B

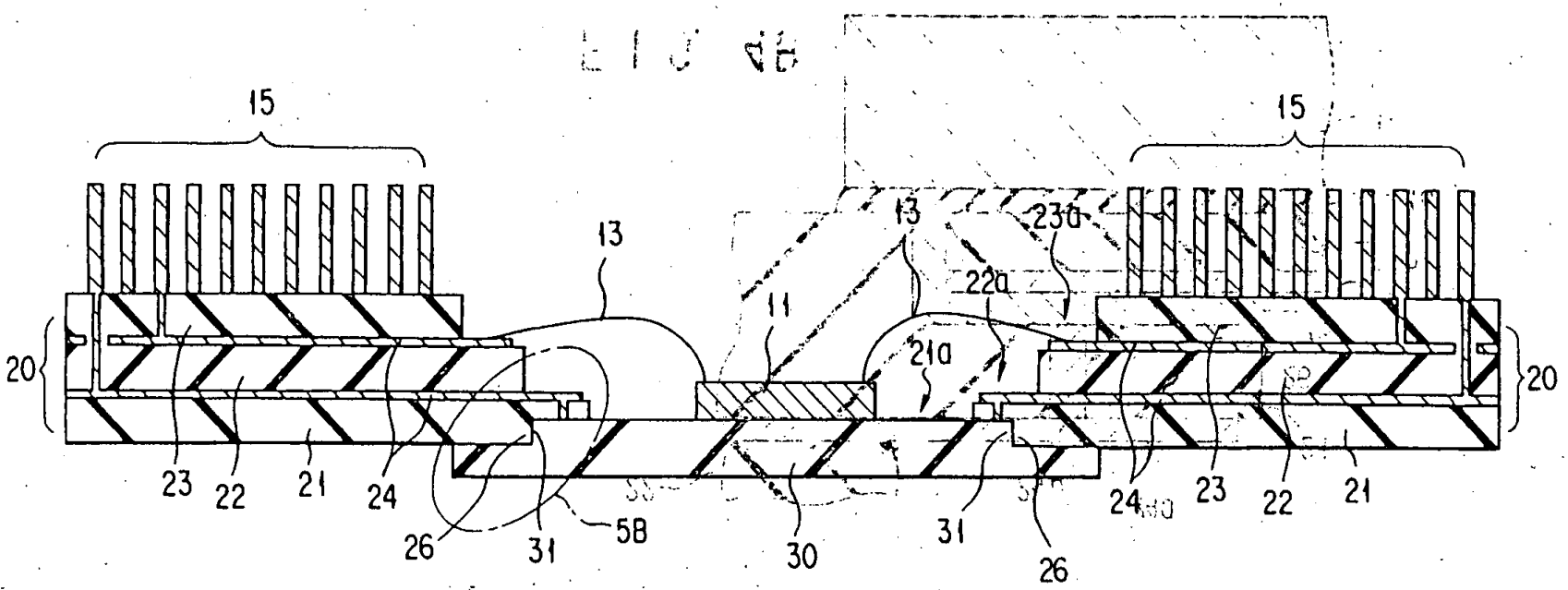


FIG. 5A

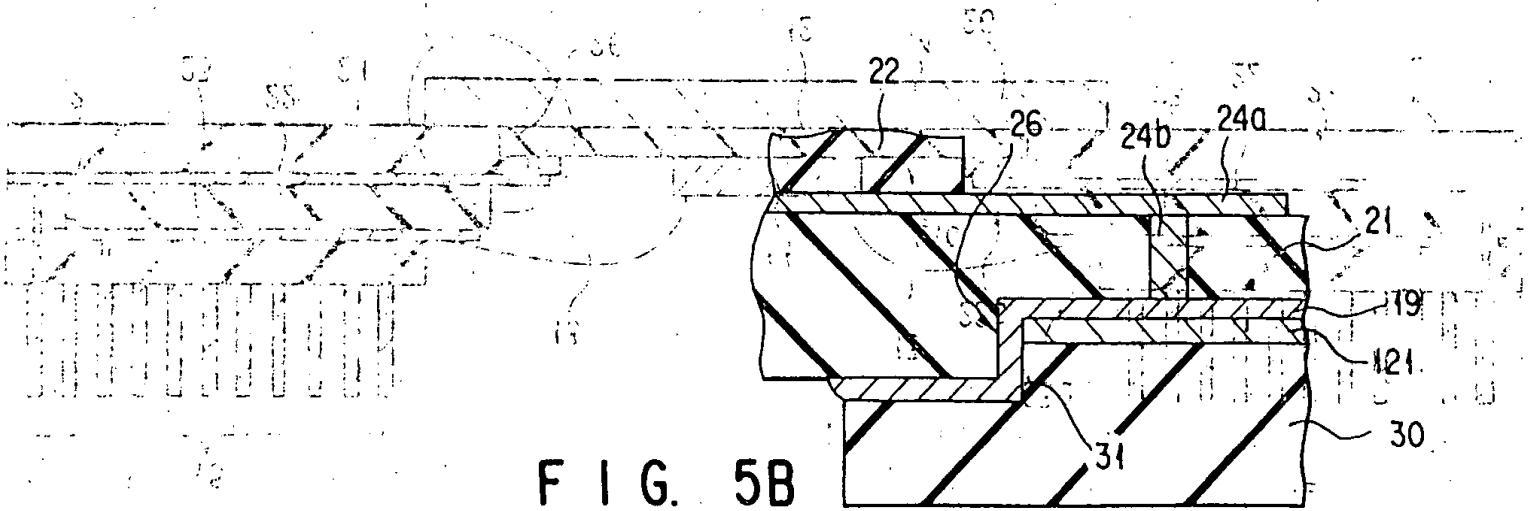


FIG. 5B

EP 0 643 811 A2

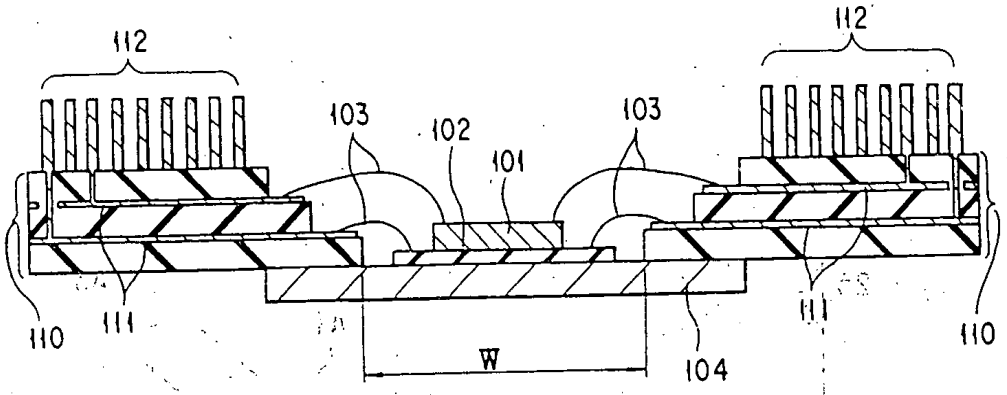

112
112
103
102
103
101
110
111
111
110
W
104

FIG. 6

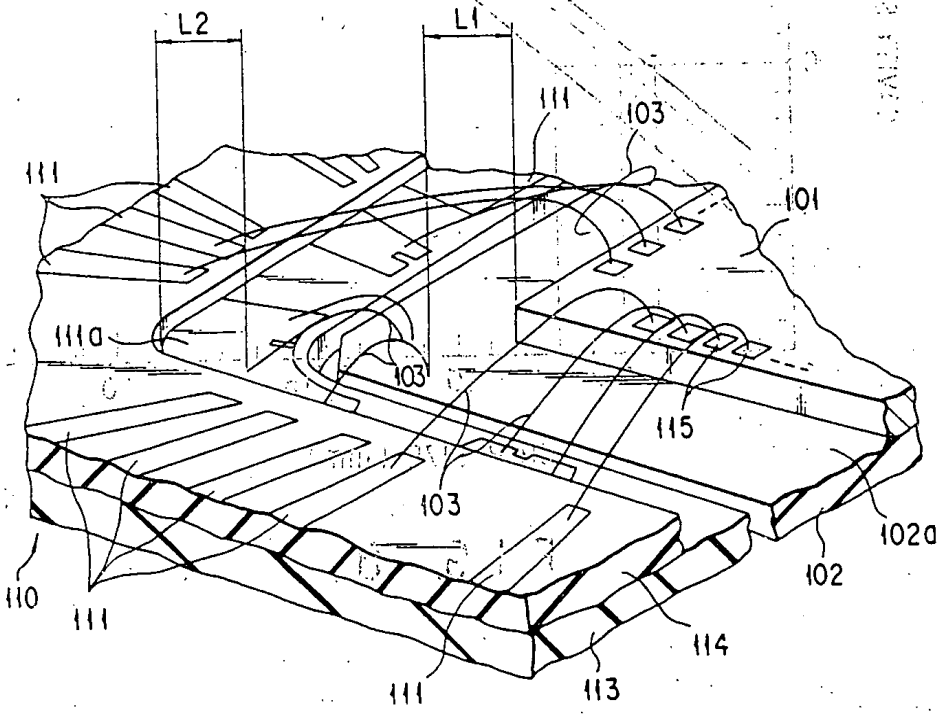

L2
L1
111
103
111
101
111a
103
115
103
102a
102
110
111
114
111
113

FIG. 7

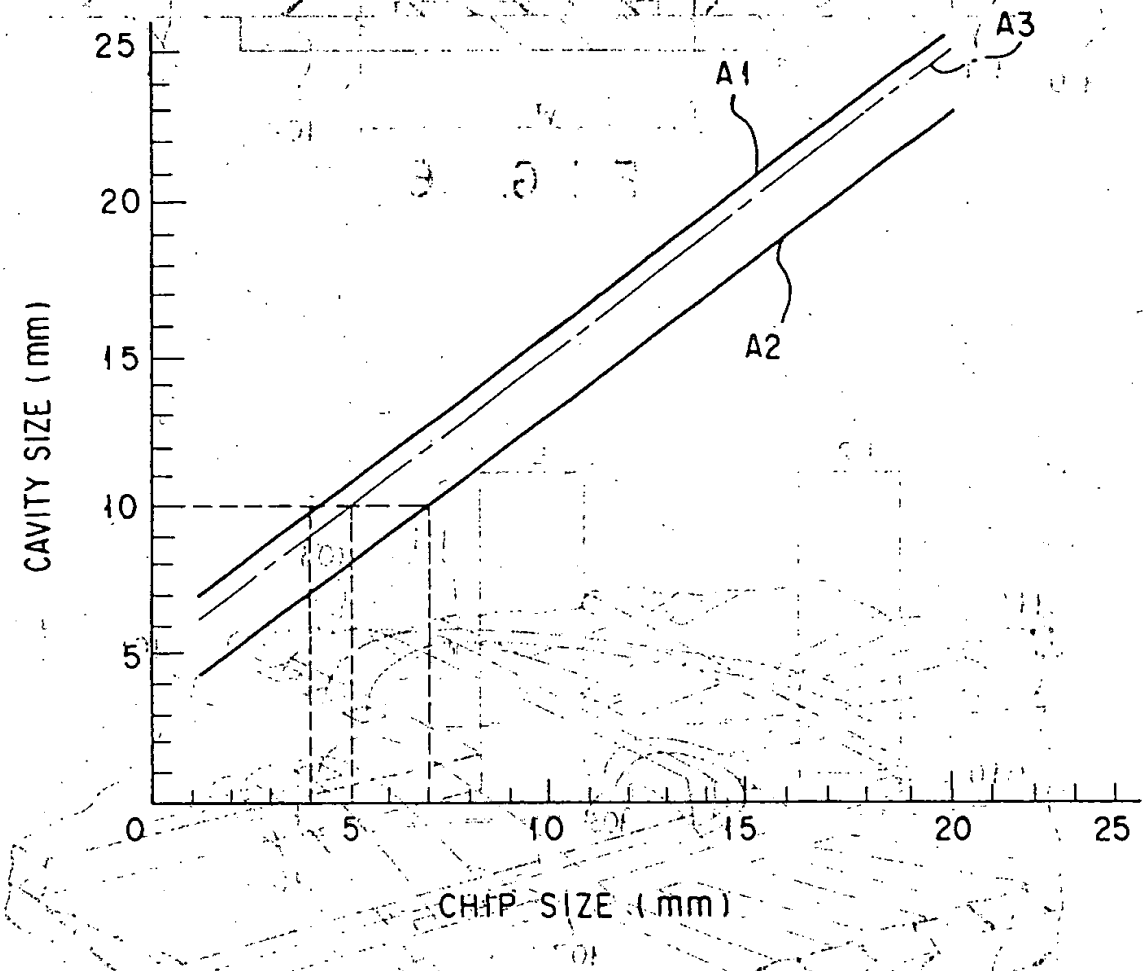


FIG. 8

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 645 811 A3**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **94115009.6**

(22) Date of filing: **23.09.94**

(51) Int. Cl.[6]: **H01L 23/057**, H01L 23/367, H01L 23/50, H01L 23/498

(30) Priority: **24.09.93 JP 238144/93**

(43) Date of publication of application: **29.03.95 Bulletin 95/13**

(84) Designated Contracting States: **DE FR GB**

(88) Date of deferred publication of the search report: **20.09.95 Bulletin 95/38**

(71) Applicant: **KABUSHIKI KAISHA TOSHIBA**
72, Horikawa-cho,
Saiwai-ku
Kawasaki-shi,
Kanagawa-ken 210,
Tokyo (JP)

(72) Inventor: **Kozono, Hiroyuki, c/o Intellectual Property Div.**
Kabushiki Kaisha Toshiba,
1-1 Shibaura 1-chome
Minato-ku,
Tokyo 105 (JP)

(74) Representative: **Lehn, Werner, Dipl.-Ing. et al**
Hoffmann, Eitle & Partner,
Patentanwälte,
Arabellastrasse 4
D-81925 München (DE)

(54) Semiconductor device having semiconductor chip with backside electrode.

(57) A semiconductor chip (11) is mounted on a chip-mounting section (12). A conduction path forming section (20) having a plurality of conduction paths (24) formed therein is placed around the chip-mounting section (12). A heat sinking board (14) is bonded to the backsides of the chip-mounting section (12) and the conduction path forming section (20). In the conduction path forming section (20), a second insulating layer (22) is formed with notches (25), whereby the exposed area of conduction paths (24) that are wire-bonded to the chip-mounting section (12) is increased.

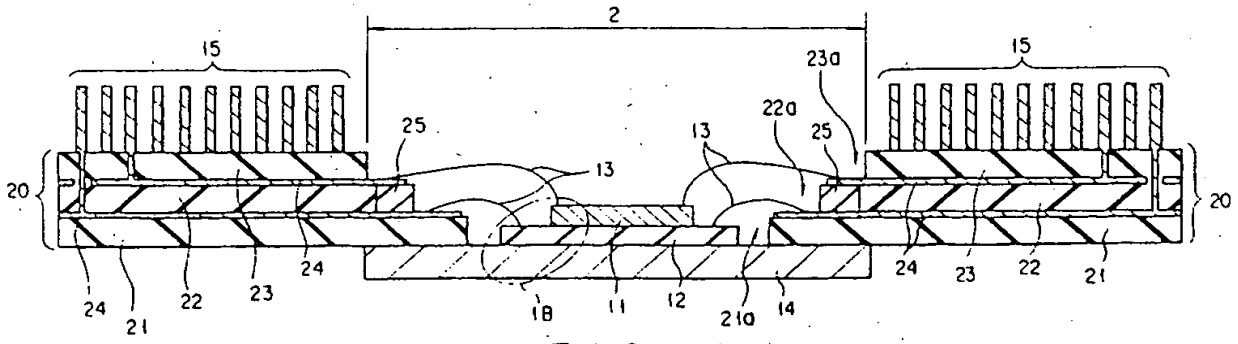


FIG. 1A

EP 0 645 811 A3

European Patent Office

EUROPEAN SEARCH REPORT

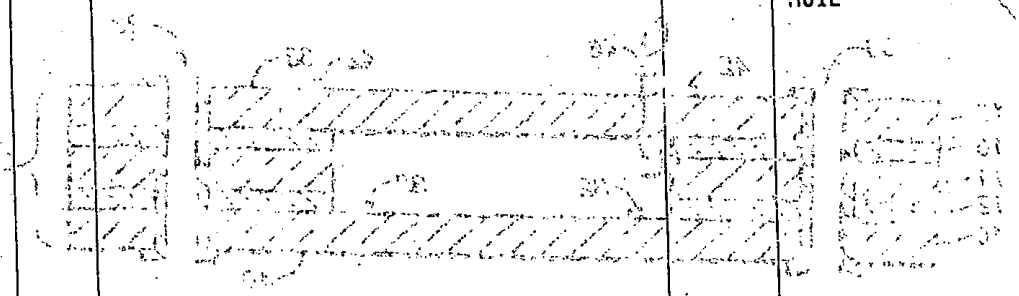
Application Number EP 94 11 5009

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	EP-A-0 416 726 (ADVANCED MICRO DEVICES) * abstract; figures 1,5-7 * ---	1-3 5,6	H01L23/057 H01L23/367 H01L23/50 H01L23/498
X Y	US-A-4 513 355 (SCHROEDER ET AL.) * abstract; figures 1,2,4,5 * ---	4,7 5,6	
X	40th IEEE/ECTC, 1990, Las Vegas, Nevada, T. MIYAGI ET AL.: "GaAs Multichip Module for a Parallel Processing System", pp. 580-585 * figure 10 * ---	4	
A	39th IEEE/ECC, May 22-24, 1989, Houston, Texas, D. QUINT ETAL.: "Electrical Design Methodology of a 407 Pin Multi Layer Ceramic Package", pp. 392-397 * figure 4 * -----	1-7	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L



The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 July 1995	Prohaska, G

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)